

REMARKS

Claim 7 has been cancelled. Claims 1-3, 6 and 8-12 have been amended. Claims 1-6 and 8-12 remain for further consideration. No new matter has been added.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The marked-up version of the changes begin on the page captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE"

The rejections shall be taken up in the order presented in the Official Action.

1. A proposed drawing amendment is attached herewith labeling FIGs. 1 and 2 as prior art.
2. The disclosure currently stands objected to since there is no label 21' in FIG. 2, and no reference number 42 in FIG. 5.

FIG. 2 has been amended to include label 21'. Examiner is authorized to remove "42" from the specification.

3. It is respectfully submitted that the specification contains a proper written description of the invention. See *Dental Prodx LLC v. Advantage Dental Products Inc.*, Fed. Cir. Docket # 02-1107, October 25, 2002.

not OK It is alleged that the "*written description never discloses the terminal [40] is connected to a circuit [4] that is being protected as claimed in claim 6.*" (Official Action, pg. 2). It is respectfully submitted this is disclosed, inter alia, on page 12, lines 12-15 of the specification.

not ok It is also alleged "*written description never discloses the claimed subject matters as claimed in claims 8-11.*" (Official Action, pg. 2). It is respectfully submitted this subject matter is disclosed, inter alia, on page 12, lines 12-15 of the specification.

4. Claims 9-11 currently stand rejected under 35 U.S.C. §112, second paragraph for allegedly failing to particularly point and distinctly claim the subject matter deemed to be the subject matter of the present invention.

Claims 9-11 have been amended.

5-6. Claims 1-4 and 12 currently stand rejected for allegedly being anticipated by U.S. Patent 6,172,404 to Chen (hereinafter "Chen").

Claim 1 has been amended to recite that the lateral thyristor structure comprises at least two lateral thyristors. Chen discloses only a single lateral thyristor structure. A 35 U.S.C. §102 rejection requires that a single reference teach each and every element of the claimed invention. Chen fails to disclose at least two lateral thyristors, wherein each includes the structure as recited in claim 1. Hence, Chen is incapable of anticipating the claimed invention.

Claim 12 has been amend to recite that the lateral thyristor structure is symmetrical and comprises at least two lateral thyristors. Again, Chen fails to disclose at least two lateral thyristors, which each include the structure as recited in claim 12. Hence, Chen is incapable of anticipating claim 12.

7-8. Claims 5-7 currently stand rejected for allegedly being obvious in view of the subject matter disclosed in Chen.

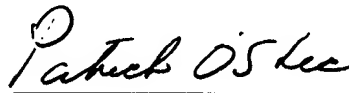
It is respectfully submitted that this rejection is now moot since claim 1 is patentable for at least the reasons set forth above.

Since claims 5-8 have not been rejected in view of prior art, it is presumed these claims contain allowed subject matter, and will be allowed once the issue of the written description is resolved.

For all the foregoing reasons, reconsideration and allowance of claims 1-6 and 8-12 is respectfully requested.

If a telephone interview could assist in the prosecution of this application, please call the undersigned attorney.

Respectfully submitted,

A handwritten signature in cursive script, reading "Patrick O'Shea", is written over a horizontal line. To the right of the signature is a large, stylized checkmark.

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VERSION WITH MARKINGS TO SHOW CHANGES MADE TO THE CLAIMS

Cancel claim 7.

Amend claims 1-3, 6 and 8-12 as follows:

1. (amended) A lateral thyristor structure for protection against electrostatic discharge, comprising:

at least two lateral thyristors, which each include

a semiconductor substrate [(20)] of a first conduction type, with a surface;

a well region [(21)] of a second conduction type, opposite to said first conduction type, which is introduced into said surface of said semiconductor substrate;

a first strongly doped region [(22)] of said second conduction type that is introduced into said surface of said semiconductor substrate [(20)] and is electrically connected to a first terminal [(26)];

a second strongly doped region [(23)] of said first conduction type that is introduced into said well region [(21)] and is electrically connected to a second terminal [(27)];

a third strongly doped region [(24)] of said second conduction type, which is introduced into said well region [(21)], is electrically connected to said second terminal [(27)], and is spatially arranged between said first strongly doped region [(22)] and said second strongly doped region [(23)]; and

a fourth strongly doped region [(25)] of said second conduction type, which is introduced into said surface of said semiconductor substrate [(20)] and into said well region [(21)], and is spatially situated above a pn junction that is formed between said semiconductor substrate [(20)] and said well region [(21)], and between said third strongly doped region [(24)] and said first strongly doped region [(22)].

2.(amended) The lateral thyristor structure of claim 1, comprising a field oxide region [(28)] that is situated between said first strongly doped region [(22)] and said fourth strongly doped region [(25)].

3.(amended) The lateral thyristor structure of claim 1, comprising a field oxide region [(29)] that is situated between said second strongly doped region [(23)] and said fourth strongly doped region [(25)].

6.(amended) The lateral thyristor structure of claim 5, comprising a region [(41)] of said second conduction type, and including a terminal [(40)] that is introduced into a field oxide region [(29, 30)], wherein said terminal [(40)] is connected to a circuit [(4)] that is being protected.

8.(amended) The lateral thyristor structure of claim [7]6, wherein said least two lateral thyristors [component structures] are surrounded by a substrate contact ring [(31)].

9.(amended) The lateral thyristor structure of claim [7]6, wherein said least two lateral thyristors [component structures] are arranged symmetrically, and in such that said [active]

doped regions adjoin one another closely, while said substrate contacting ring is removed as far as possible from said active region.

10.(amended) The lateral thyristor structure of claim [7]6, wherein said [active] doped regions adjoin one another closely, while said substrate contact ring is removed as far as possible from said [active region] doped regions.

11.(amended) The lateral thyristor structure of claim [7]6, wherein said least two lateral thyristors [component structures] are arranged symmetrically, and [in] such that said [active] doped regions adjoin one another closely, while said substrate contacting ring is removed from said [active] doped regions.

12.(amended) A symmetrical lateral thyristor structure for protection against electrostatic discharge, comprising:

at least two lateral thyristors, which each include

a semiconductor substrate of a first conduction type, with a surface;

a well region of a second conduction type, opposite to said first conduction type, which is introduced into said surface of said semiconductor substrate;

a first strongly doped region of said second conduction type that is introduced into said surface of said semiconductor substrate and is electrically connected to a first terminal;

a second strongly doped region of said second conduction type that is introduced into said well region and is electrically connected to a second terminal;

a third strongly doped region of said second conduction type, which is introduced into said well region, is electrically connected to said second terminal, and is spatially arranged between said first strongly doped region and said second strongly doped region; and

a fourth strongly doped region of said second conduction type, which is introduced into said surface of said semiconductor substrate and into said well region, and is spatially situated above a pn junction that is formed between said semiconductor substrate and said well region, and between said third strongly doped region and said first strongly doped region.